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A New GaN/SiC Transistor Digitizer

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plug & play instruments
oscilloscopes

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Ken Henderson is a hardware engineer at Cleverscope (New Zealand), has a Masters in Electrical Engineering, and has been active in the industry for more than 30 years.
Ken has designed variable speed drives for GEC (an English company), and has had long exposure to the design, and measurement of power electronic systems.

Bart Schroder
Cleverscope, New Zealand
Is an Engineer, and has been active in the industry for forty years.

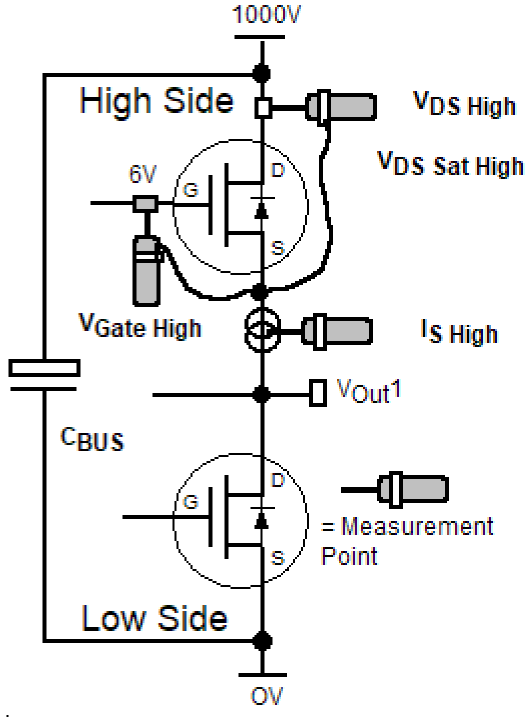
Why are we doing this?

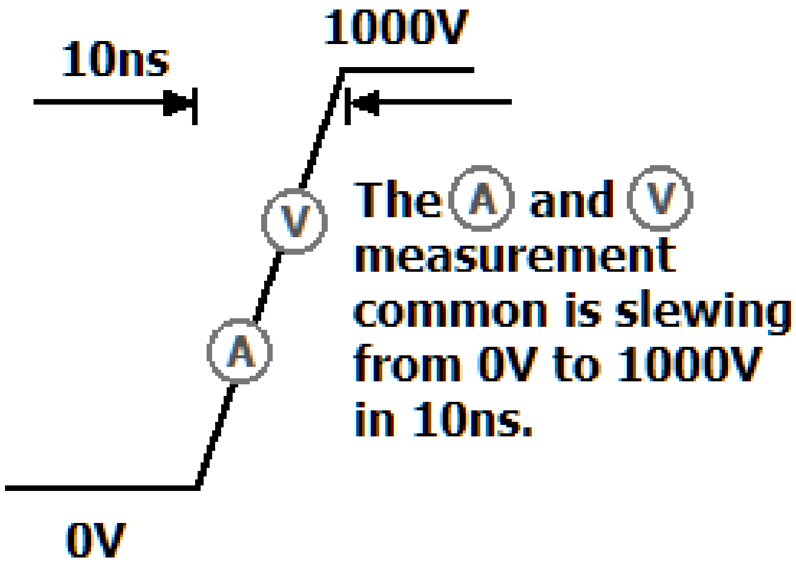
To do design verification and measure power loss in GaN/SIC FET UUTs.

And do this while the common slews at 100V/ns.

Actions:

- Measure V_{DS}, $V_{DS\ Sat}$, I_S, V_G for transistor on the high or low side.
- Use these values to calculate transistor loss, bus loop inductance, bus loop capacitance, Gate drive performance, parasitic signals, and EMC – Everything!





The Ⓐ and Ⓥ measurement common is slewing from 0V to 1000V in 10ns.

Ⓥ = Voltage Measurement

Ⓐ = Current Measurement

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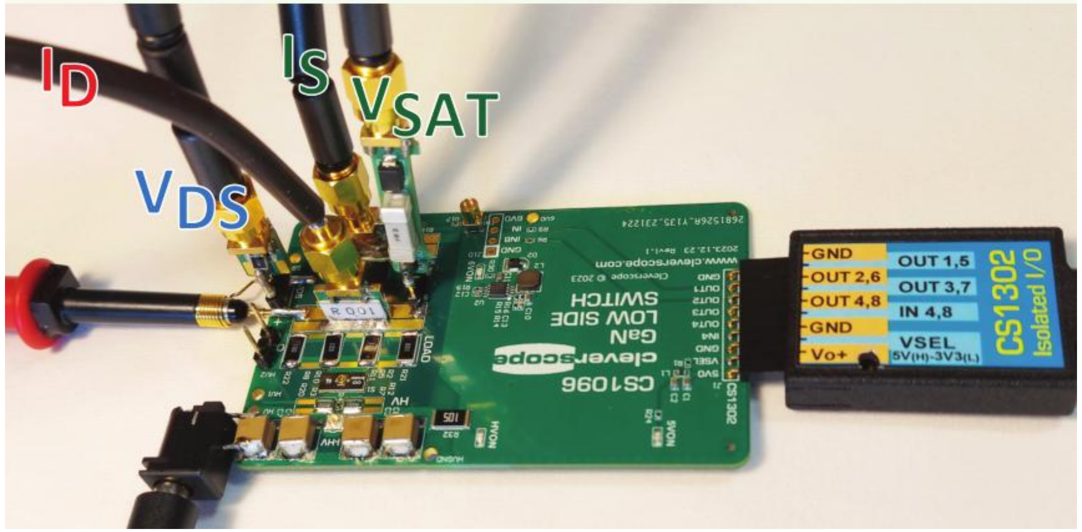
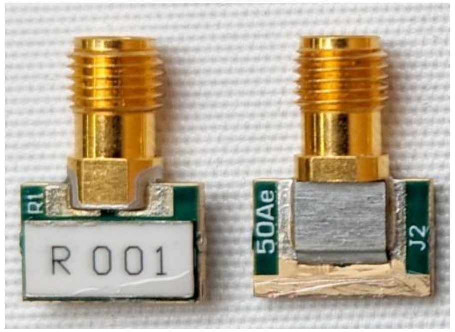
The work that has come before

The CS1202 builds on fiber optic isolated products that we have already developed:

- The CS1200 Isolated Voltage Digitizer (VD) for V_{DS} and V_{GS} measurement.
- The CS1201 Isolated Current Digitizer (CD) and CS1501 1GHz current shunt for I_S measurement.
- The CS1133 Isolated V_{SAT} probe for clipped voltage measurement of the On transistor/diode with 1mV resolution.
- The prototype CS1202 Isolated V_{DS}, V_{SAT}, I_S digitizer including hardware Power and Energy measurement





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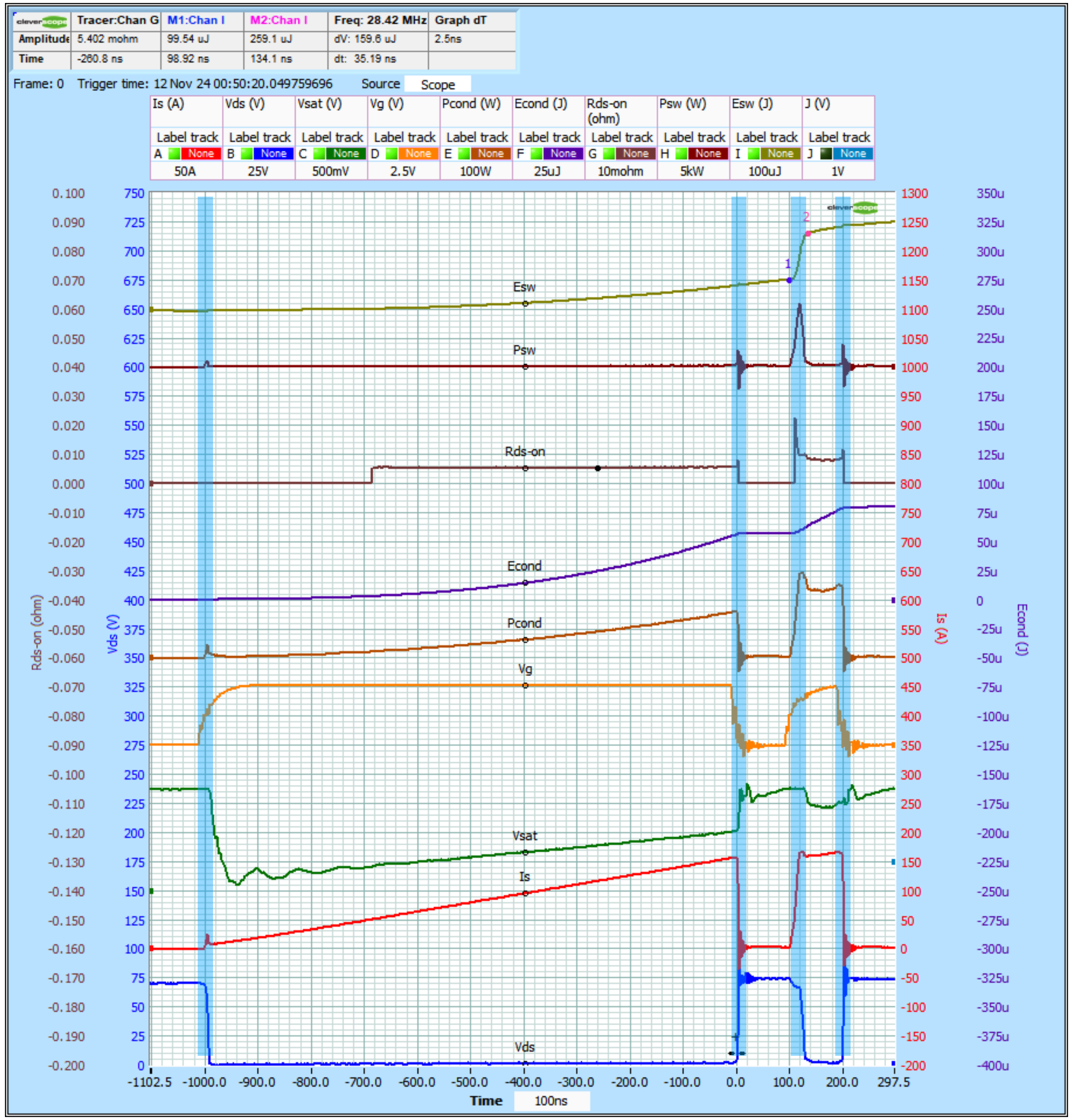
The Justification work - 1

Things we realized:

- There is a lot of slow moving signal – why digitize it at 5 GSPS, it will only cost more Power and $$$
- This whole business is about efficiency, which means you have to measure loss.
- Doing DPT is all very well, but we also have to measure losses over many seconds to get the full picture.

= Fast edges, digitize at 5 GSPS.

Everything else at 250 MSPS



	Tracer:Chan G	M1:Chan I	M2:Chan I	Freq: 28.42 MHz	Graph dT
Amplitude	5.402 mohm	99.54 uJ	259.1 uJ	dV: 159.6 uJ	2.5ns
Time	-260.8 ns	98.92 ns	134.1 ns	dt: 35.19 ns	

Frame: 0 Trigger time: 12 Nov 24 00:50:20.049759696 Source Scope

Is (A)	Vds (V)	Vsat (V)	Vg (V)	Pcond (W)	Econd (J)	Rds-on (ohm)	Psw (W)	Esw (J)	J (V)
Label track	Label track	Label track	Label track	Label track	Label track	Label track	Label track	Label track	Label track
A None	B None	C None	D None	E None	F None	G None	H None	I None	J None
50A	25V	500mV	2.5V	100W	25uJ	10mohm	5kW	100uJ	1V

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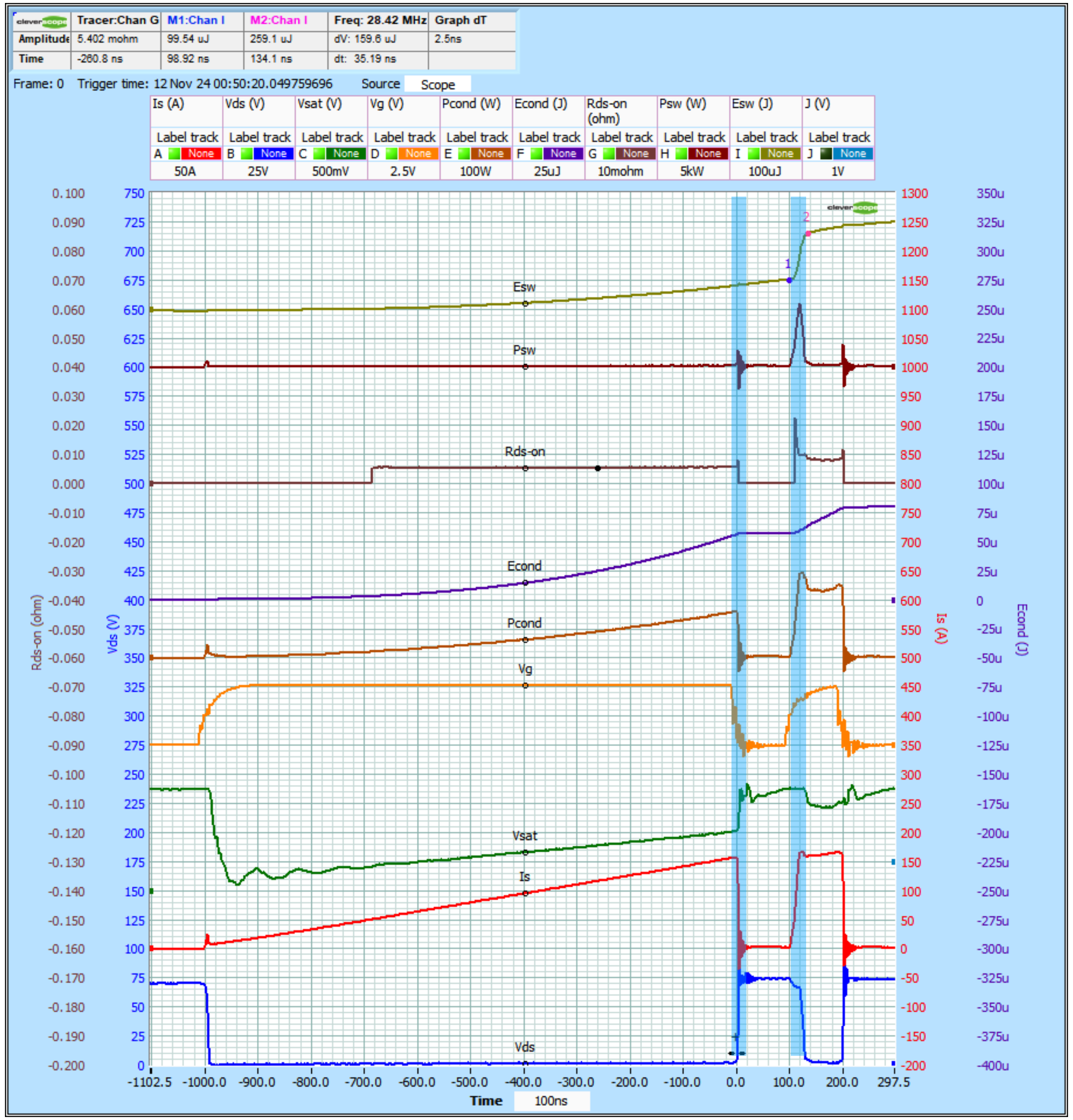
The Justification work - 2

We have chosen two use cases:

- DPT use – the 2nd and 3rd edges are the ones that matter. We want to measure loss, bus loop inductance, transistor capacitance, gate drive and resonances.
- Continuous (up to days) use – show power and energy loss distribution over multiple output cycles, measure total power loss per second. Take fast snapshots every 50msecs.

Once and X 100k/sec



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50A	25V	500mV	2.5V	100W	25uJ	10mohm	5kW	100uJ	1V

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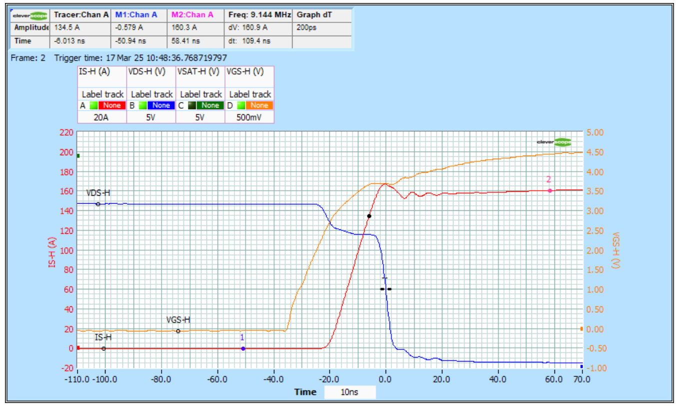
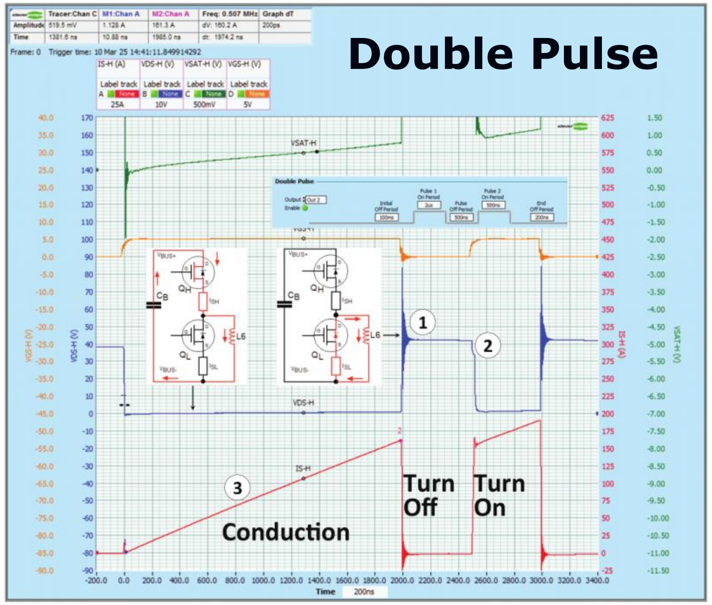
Use Case 1: DPT

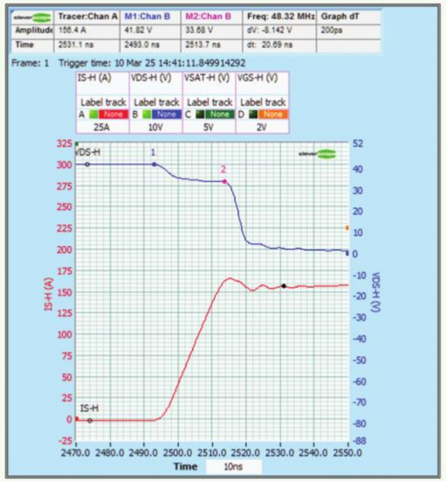
VGS in relation to VDS, IS



Double Pulse



Bus Loop Inductance: 914pH ②

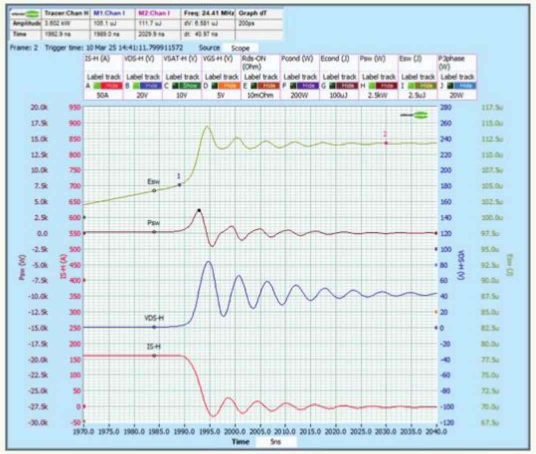


QH R_{DSON}: 5mΩ ③

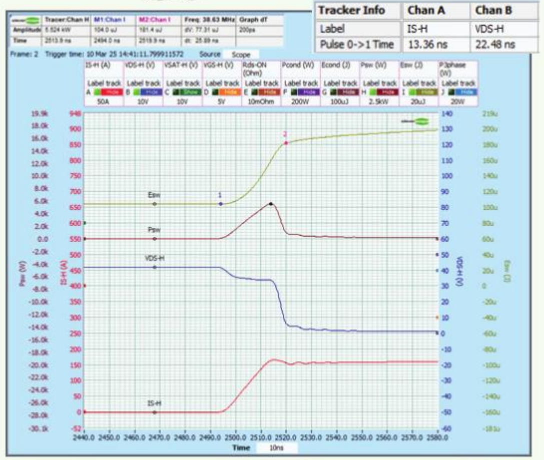
Maths:

Check	Equations	Used?	Process	Destination
●	c/a*(gtz(a-40))	●	----->	e

QH turn off ① energy: 6.58uJ



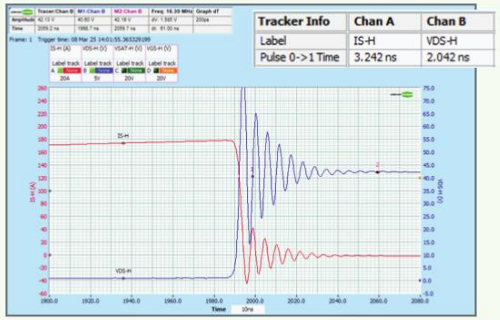
QH turn on ② energy: 77.31uJ



Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	13.36 ns	22.48 ns

QH conduction ③ energy: 77.31uJ

QH Output ① capacitance: 908 pF I_S fall: 3.2ns V_{DS} rise: 2.0 ns



Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	3.242 ns	2.042 ns

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Use Case 2: Continuous Capture

Using the Cleverscope 3MSPS/8 channel streaming interface continuously calculate and transfer these values for the next edge:

- Δt from the last edge to this edge
- $E_{CONDUCTION}$ for this period
- $R_{DS\ ON}$ for this period
- P_{SW} Peak for this edge
- E_{SW} for this edge

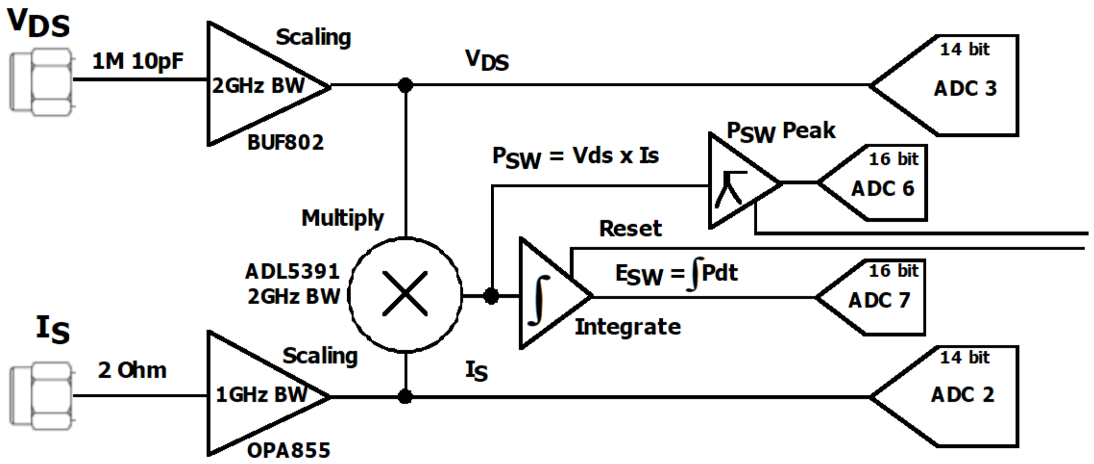
Then continuously display:

- A graph of the pulse width distribution
- Conduction Watts in seconds from $E_{CONDUCTION}$
- Switching Watts in seconds from E_{SW}
- Graph total power loss as it happens with user definable time resolution.
- Graph the $R_{DS\ ON}$ distribution

Measuring P_{sw} and E_{sw}

We calculate PSW and ESW in hardware. The advantages are:

- The 2 GHz multiplier does not have digitization error.
- The Energy Integrator and Power Peak Capture are analog and are digitized in slow time. No fast ADC is required.



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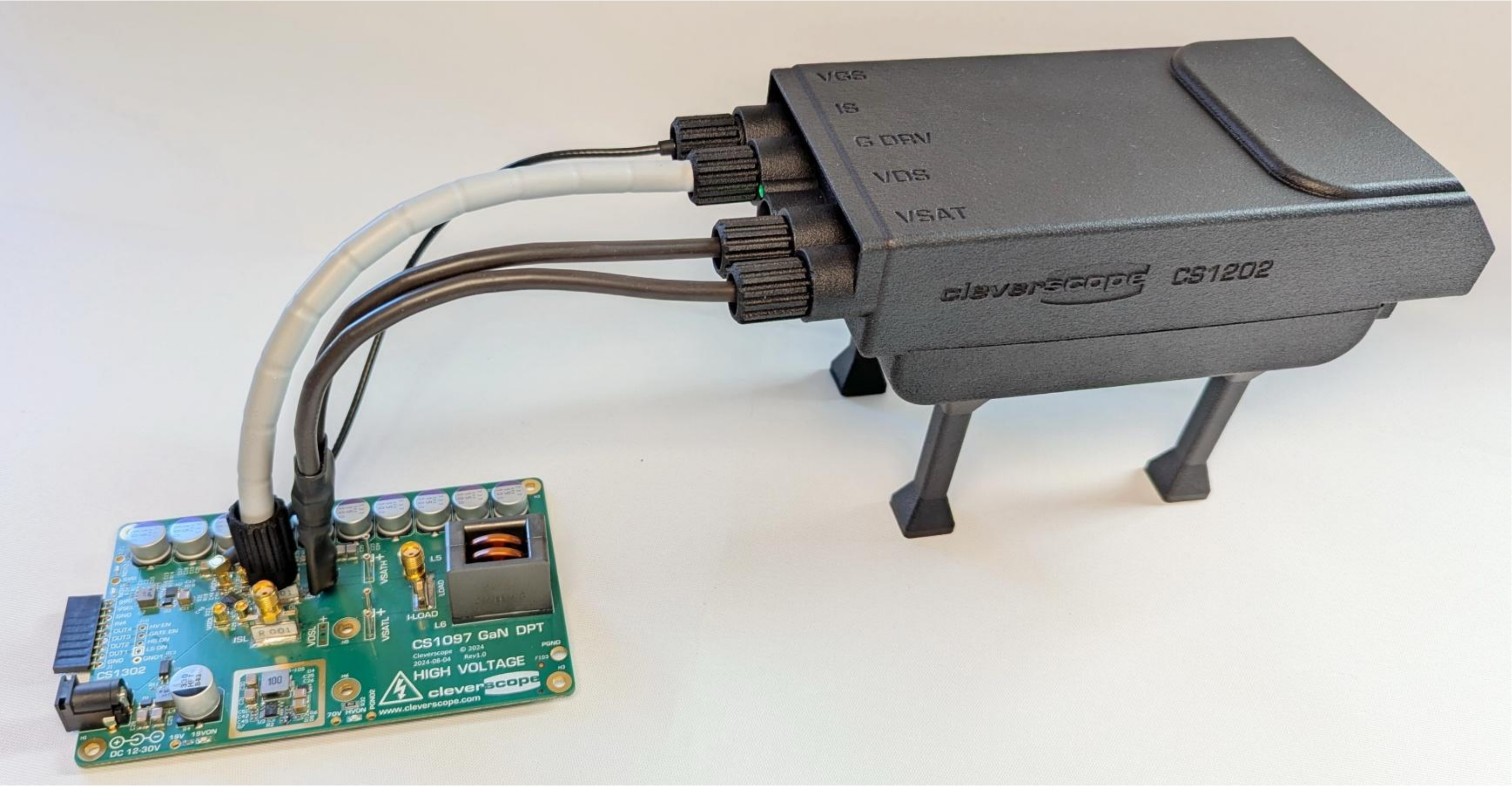
After all our justification work, this is the design we have come up:



Key Parameters to meet:

- Doesn't cost too much!
- Doesn't use too much power
- Can fully characterize transistor operation in a double pulse test (DPT)
- Can continuously measure loss.
- Bandwidth of 1GHz and 5GSPS when it matters.
- Insertion inductance of 160pH
- Resolution of 1 part in 1000

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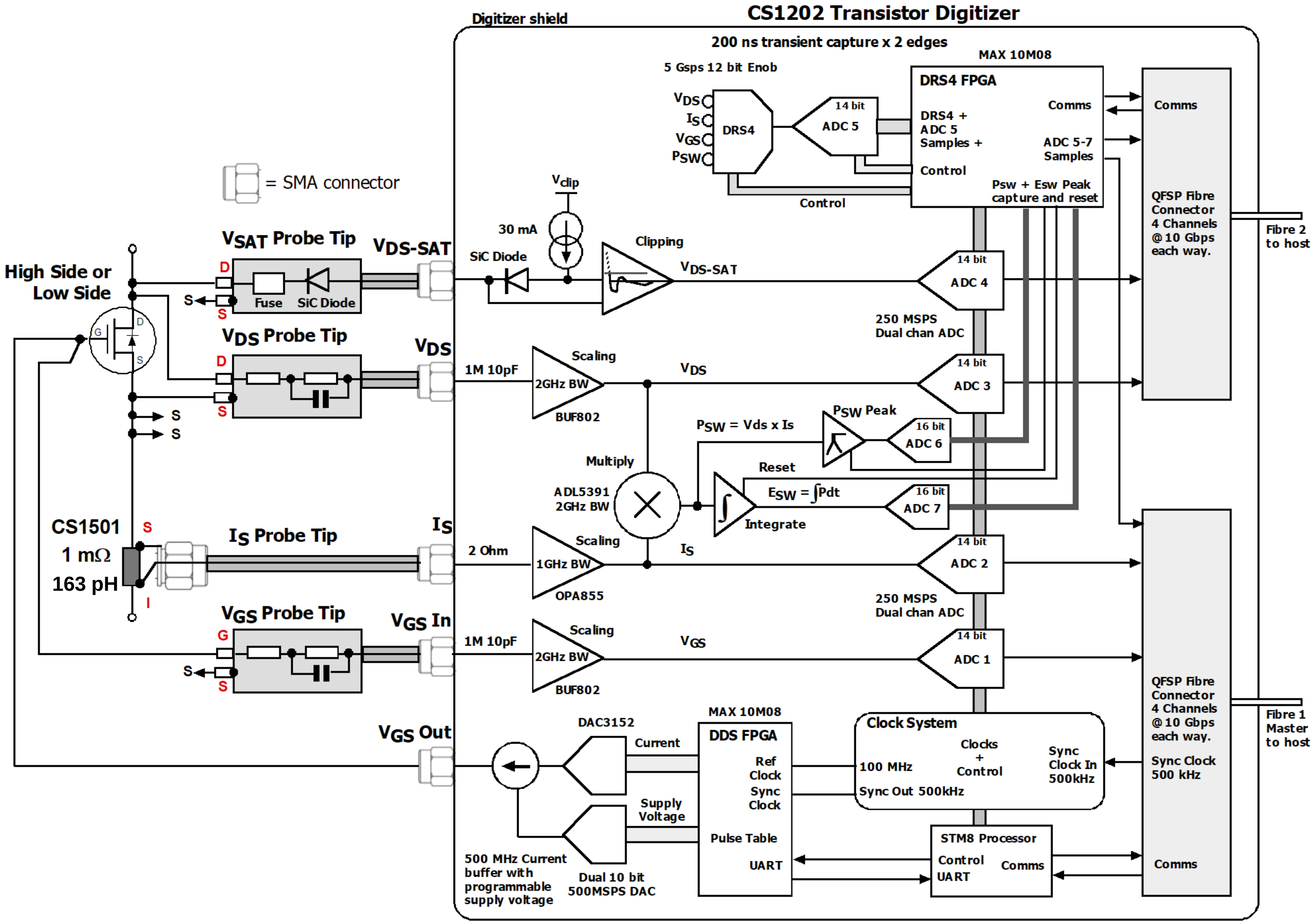

A Diagram of all the parts

7 ADCs capture:

- VDS *
- VDS-SAT
- IS *
- Vgs In *
- Psw *
- Psw peak
- Esw

* Capture at 250 MSPS and 5 GSPS on the edge

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Capturing the edge at 5GSPS

Our design uses a DRS4 switched capacitor array to capture the transient. We can simultaneously capture 4 channels for 200 ns on every edge. These are the channels:

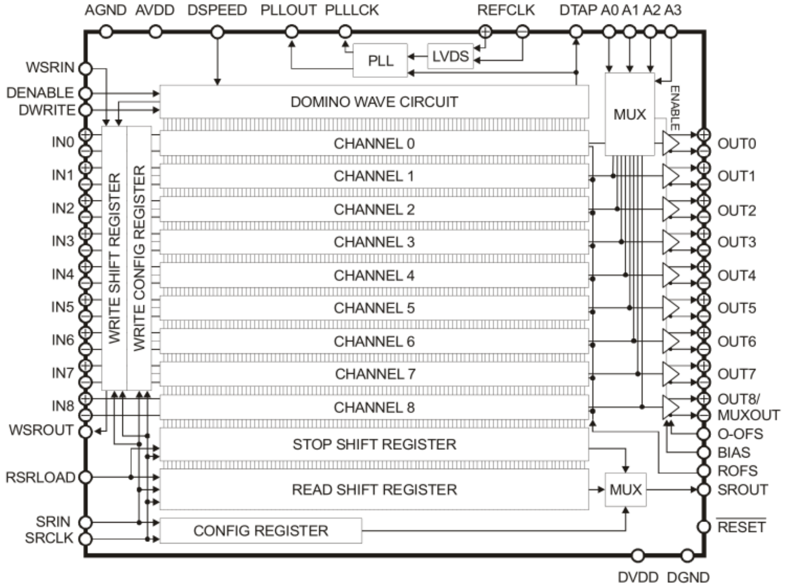
- V_{DS}
- I_S
- V_{GS}
- P_{SW}

After capture we time stamp the samples and send them back to the PC for further processing:

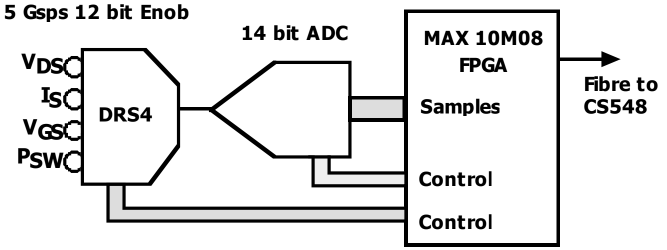
- Scale and Offset correction
- Super-imposition onto the 250 MSPS sample stream in the right place
- The signals are graphed as normal.

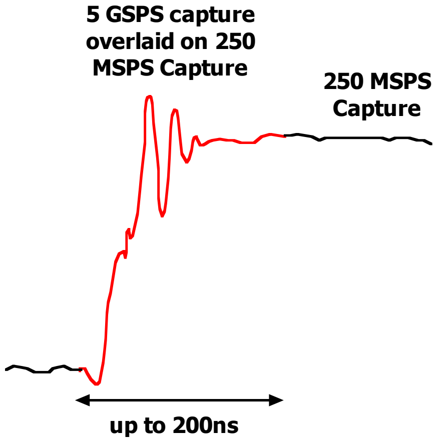
Measuring at 5GSPS

The DRS4 chip



5GSPS 200ns edge capture digitizer





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Conclusion

We are developing a fully integrated GaN transistor digitizer including:

- Isolated using fibre optic - increased safety and CM voltage of many kV
- Completely Shielded to reduce Common Mode current distortion > 140 dB CMRR
- Reduce common mode current with CM chokes to reduce load on UUT
- Digitize in probe to reduce noise – 1 part in 1000 resolution, 8x better than others
- Current sensor: measures DC, high BW, low insertion inductance of 163 pH
- Includes hardware calculation of P_{SW} and E_{SW}, and continuous recording of each edge loss.
- Includes 5 GSPS transient digitizer with 200ns capture window and 12 bit effective number of bits (ENOB).

The CS1202 Transistor Digitizer will offer a low-cost method to characterize the switching transistor, with an accuracy and performance not currently available.

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ATLANTA,USA

Thank you for the attention!

Visit us at booth 1751.

I‘m pleased to answer your questions:
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